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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,822	03/06/2002	Kenji Furuya	1614.1221	5676

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,822	FURUYA ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozuyama (5,862,359).

With regard to claim 1, Nozuyama discloses a semiconductor device (10, for example) comprising: a plurality of function blocks (13, 14, 15, and 16, for example); a plurality of buses (22, 23, for example), each of which is respectively connected to one of the plurality of function blocks (13, 14, 15, 16); a plurality of control signal lines (EN12-EN31, see also column 6, lines 1-46), each of which is respectively connected to one of the plurality of function blocks (13-16); a main bus (21, connected to CPU 11); a bus control unit (CPU 11) connected to the main bus (21); a bus division control unit (including 3 and 4) located between the plurality of buses and the main bus (21), for connecting one of the plurality of buses (22, 23) to the main bus (21) and transmitting a control signal to a corresponding one of the plurality of control signal lines (EN12-EN31, see also column 6, lines 1-46) in accordance with a decoded result of information supplied from the bus control unit via the main bus (21), thereby controlling a corresponding one of the plurality of function blocks and controlling communication between at least two functional blocks (see at least column 3, lines 18-23; column 7,

lines 10-19). It is also clear that the signal lines in Nozuyama are separate from one another.

With regard to claim 2, the bus division control unit comprises: a decoder unit (4) for decoding the information supplied from the bus control unit (11) via the main bus (21) and generating the control signal; and a bus dividing unit (see Figs. 2A/2B, column 6, lines 1-46) for connecting one of the plurality of buses to the main bus, in accordance with a decoded result of the decoder unit.

With regard to claim 3, the bus division control unit (including 3 and 4) connects one of the plurality of buses (22, 23) to the main bus (21), in accordance with a decoded result of address information (address of the functional unit that the CPU needs to access must be always provided by the CPU) transmitted from the bus control unit via the main bus (see at least column 3, lines 18-23; column 7, lines 10-19).

With regard to claim 4, at least two of the plurality of function blocks (13, 14, for example) shares one (22, for example) of the plurality of buses, and the bus division control unit (including 3 and 4) controls a transfer operation between the two function blocks (13, 14) via the one (22) of the plurality of buses in response to a transfer request signal.

With regard to claim 5, it is clear that the bus division control unit (including 3 and 4) simultaneously transmits a write-enable signal to one of the two function blocks and a read-enable signal to the other one of the two function blocks (in Nozuyama, as discussed above, the communication, i.e., read/write, between functional blocks 13 and 14 is enabled by an enable signal from bus switch 3; blocks 13 and 14 receive the

signal simultaneously and one of the functional blocks (13, 14) reads the other one of blocks (13, 14) writes.

With regard to claim 6, it is clear that in order to enable communication between the blocks (13, 14, for example), the source (either 13 or 14) and the destination (the other of 13 or 14) must be specified/determined.

With regard to claim 7, as in any master/initiator and slave/target relationship, in Noyuyama, the CPU has to send request access (by specifying the address of the target or functional unit) for processing before the actual transfer request may be processed by the bus division control unit including the bus switch 3 and the decoder 4.

With regard to claim 8, it is clear that when access request to blocks 13, 14, for example is granted and transfer is processed, the CPU 11 can make another access request to functional blocks 15 and 16 while the transfer is in progress.

With regard to claim 9, in Nozuyama, the CPU can make either a READ or WRITE request to the functional blocks, and the bus switch (3) and decoder (4) must be able to recognized the type of request in accordance to the principle of computer architecture so that a suitable communication direction between the CPU and the plurality of functional blocks can be performed.

With regard to newly added claim 11, see discussion above, since these newly presented claims, as drafted, are even broader than the originally presented claims. Therefore, no further explanation/argument is deemed necessary.

Noyuzama does not disclose that the "control signal line is not connected to two or more functional blocks."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ one instead of two or more functional blocks for each divisional bus, since the use of one functional block instead of two or more functional blocks for each divisional bus is only a matter of design choice. In any event, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ one instead of two or more functional blocks for each divisional bus, since the use of one functional block instead of two or more functional blocks for each divisional bus is old and well-known as evidenced from Wertheim (previously cited); and using one instead of two or more functional blocks in for each divisional bus in Nozuyama only involves ordinary skill in the art.

Response to Arguments

Applicants' arguments filed 4/19/2005 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997).* In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read

into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

Applicants' argument regarding the newly added limitation, "the control signal line is not connected to two or more functional blocks" is moot in view of the new ground of rejection set forth above.

Applicants argue that "Nozuyama teaches a decoder 4 that is an instruction decoder for decoding instruction signals, and that does not decode address information, as is recited in amended claim 1 of the present invention." Contrary to Applicants' argument, in Nozuyama, a decoder 4 is provided, which serves to a control signal (supplied from the CPU, for example) which requires 2 of the divisional buses 21-23 in the operation of the transfer bus, and control the bus switch circuit such that only the divisional buses are connected to each other at one place on the basis of the decoded output. See column 3, lines 18-23, and column 7, lines 10-19. Note that as in any master/initiator and slave/target relationship, in Noyuyama, the CPU has to send request access by specifying the address of the target or functional unit for processing before the actual transfer request may be processed by the bus division control unit including the bus switch 3 and the decoder. It is clear that the addresses of the

functional units connected to 2 of the divisional buses 21-23 that the CPU needs to access must be always provided by the CPU and decoded by the decoder 4 to allow connections to the functional units via 2 of the divisional buses connected to each other. For example, as illustrated in the acknowledged prior art of Fig. 1, the address of functional blocks 12 must be always decoded by the decoder+latch so that only the functional block that has the address matched the address specified by the control unit can establish communication with the control unit. Another example is the disclosure of Werthheim et al., cited as relevant art in the previous Office Action. Werthheim et al. discloses a plurality of functional blocks interconnected by a bus, a switch controller partitioning the bus into a plurality of bus segment and controlling the two of the bus segments so that the two bus segment can be interconnected or isolated in response to control information representative of the source and the destination of each bus transaction. The switch controller can also control the state of the switches to permit two or more bus transaction to be performed simultaneously. Werthheim et al. also discloses that the decoder 162 receives the address bus and control signals which indicate the source of and the destination each bus transaction. See column 5, lines 25-27, for example. Still another example is the disclosure of Foo cited below. Foo discloses an address decoder 66. See at least Fig. 5 and description thereof. In response to Applicants' argument regarding the newly added claim 11, see discussion above, since claim 11, as drafted, are even broade. Therefore, no further argument is deemed necessary. Applicants also argue that Nozuyama "fails to teach supplying a control signal to a corresponding one of the control signal lines (which are connected to

the respective function blocks) in response to a decoded result of the address information, as is recited in amended claim 1 of the present invention." Contrary to Applicants' argument, it is clear from the discussion above and at least Fig. 1 of Nozuyama that **a control signal is supplied from the CPU to a corresponding one of the control signal lines (EN12-EN31, see also column 6, lines 1-46, for example) which are connected to the functional blocks (13, 14, 15, 16, for example) in response to the output of the address decoder 4**. Further, it is clear that the control signal lines (EN12-EN31, see also column 6, lines 1-46, for example) are connected to the functional blocks.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner